SEGA OF AMERICA INC.
Consumer Products Division

32X
Hardware Manual

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History

Provisional Version 1 (May 11, 1994)

- Introduction, Sections 1 ~ 3 4, 6.2, 6.3
- Total 64 pages

Provisional Version 2 (May 23, 1994)

- Sections 3.5, 4.1 ~ 4.4, 6.1, additions
- Total 99 pages
- not created (chapter 5 Usage Examples)

Revision (1) (May 25, 1994)

- Introduction, Chapters 1 and 2
- Terminology
- Title change (Chapter 2) "32x Features" → "Configuration"
- Coordination of items (2 1, 2.2)
- Overview, Detail of features, points of caution in and after chapter 3

Revision (2) (May 30, 1994)

- Improved structure of Chapter 4
- Listed accessible blocks
- Deleted unneeded duplication between sections

Provisional Version 3 (June 1, 1994)

- "SH2 Memory Map" (Chapter 3) FIFO 2 word → 4 word
- Contents, index, etc.
- Indicated items sections 2.2, 3.3 concerning provisional version 2 But resulting applications replacing section 2.2 were lost
- Deleted entries concerning Chapter 5 (Usage Examples)
- Total 84 pages

Introduction

This manual applies to the development of game software and explains power up booster "32X" hardware functions for the MEGA Drive.

Manual Configuration

This manual is composed of the following chapters

Chapter 1 Introduction to the 32X
  Introduces the main function of the 32X

Chapter 2 Configuration
  Explains the hardware configuration and purpose of each part

Chapter 3 Functions
- 3.1 Mapping
  Explains the layout on CPU address space of each hardware part
- 3.2 Registers
  Explains the meanings of register and buffer function sequence and address, also set values
- 3.3 VDP
  Explains functions as image data formatting, screen shift, character overwrite, and Fill.
- 3.4 PWM
  Describes the PWM sound source and the PCM data play method.
- 3.5 SH2
  Explains the main CPU features and its communication with the MEGA Drive

Chapter 4 Accessing the 32X Block
  Explains about registers and buffers that can be accessed from each CPU, the method of taking access authority, and access time.

Chapter 5 Miscellaneous
- 5.1 Boot ROM
  Explains operations from when the power is turned on until executing the application.
- 5.2 Security
  Explains areas decided by previous uses of the cartridge ROM
- 5.3 Restrictions
  Explains cautionary points in creating applications

Terminology

RISC (Reduced Instruction Set Computer)

This computer architecture improves performance by simplifying instruction specifications and has simplified hardware achieving a high efficiency pipeline (parallel process of instructions within the computer).

SH2 (SH7095)

At the core of the RISC-type CPU in the Hitachi original microcomputer is a 32-bit divider and cache memory

Cache

The cache is comparatively small size high-speed memory placed between the large size low-speed memory and the CPU When data of the address to be accessed by the CPU is stored in the cache memory, it is referred to as cache hits and because the data can be accessed, the CPU can be operated at high speeds When address data of to be accessed by the CPU is not stored in the cache memory, it is referred to as cache miss The contents of the cache memory is replaced by data in the main memory

SDRAM (Synchronous Dynamic Random Access Memory)

The SDRAM differs from the typical DRAM; data of a two line address is held internally once. This is independently synchronized to the clock and transfers continuously separate from the internal DRAM operation speed

DSP (Direct Signal Processor)

Signal Processor containing a high-speed divider

DMA (Direct Memory Access)

Transfers data directly between the memory and peripheral units (I/O) or between memories without going through the CPU, usually achieved by the DMA controller (DMAC).

FIFO (First-In First-Out)

Method of outputting in the same order as inputting in the input/output operation of a buffer register or buffer memory

Master / Slave

Refers to the priority order of use authorization of a bus to which more than one processor is connected. Master takes a normal bus authorization and slave obtains permission of the master and takes bus authorization when slave bus access occurs

Contents

Chapter 1

Introduction to 32X

Chapter 1 Contents

1.1 Introduction to 32X

The 32X is a power-up booster installed in the MEGA Drive cartridge slot. This adds a bitmap screen of up to 32,768 simultaneous colors and stereo sound source that plays PCM data to the graphics and sound of the existing MEGA Drive. Two 32-bit RISC CPUs are mounted for starting screen graphics processing.

- New Screen Offered
  Frame buffer 1 Mbit DRAM x 2 (alternating draw / display)
  Maximum 32,768 colors, bitmap format
  3 mode data format
  Direct color / Packed Pixel / Run Length

  * Scroll by hardware, no sprites exist

- New Sounds Offered
  Stereo sound source that plays PCM data
  D/A conversion by a PWM modulation (11-bit resolution)

- High-Speed Microprocessor
  Two SH2 chips for the main CPU
  32-bit RISC chip with built-in process similar to DSP

- Memory
  4 Kbyte Cache memory (built into the CPU)
  2 Mbit SDRAM (main memory)

- Development Language
  C Language, Assembly Language

Chapter 2

Configuration

Chapter 2 Contents

2.1 32X Block Diagram

32X is made up of the following parts (see Figure 2.1).

- MEGA Drive I/F Component (I/F chip built-in)
- 32X Cartridge
- SH2 Component
- SDRAM (2 Mbit)
- Frame Buffer (1 Mbit X 2)
- VDP Component
- Color Palette Component (VDP chip built-in)
- PWM Component (I/F chip built-in)

These hardware resources (excluding the SH2 and SDRAM components) contained by 32X are directly controlled by the MEGA Drive 68000 CPU. The ROM cartridge can be read from both the MEGA Drive and 32X. Images and sound made by 32X are combined with images and sound made by the MEGA Drive

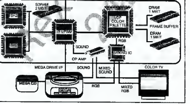

Figure 2.1 32X Block Diagram

2.2 About the 32X Block

The role and features of each 32X block shown in section 2 1 is explained below. See chapter 3 for more information

MEGA Drive I/F Component

This is an interface connecting the 32X to the MEGA Drive The 32X hardware resources (graphics, sound, and communication with SH2) and cartridge ROM are mapped through the MEGA Drive I/F in the MEGA Drive main CPU (68000) address space

32X Cartridge Component

The content of the ROM cartridge installed in the 32X cartridge slot can be read from both the 32X CPU SH2 side and the MEGA Drive side 68000 (and Z80). Nevertheless, SH2 has priority when conflict between the two exists

SH2 Component

There are two SH2 chips as main CPUs mounted in the 32X, and the cartridge ROM is connected with 32X hardware resources (graphics, sound, and communication to 68000) on a common bus. The 2 SH2 units are fixed to the master and slave by packaged conditions, the normal master gets bus authorization and slave gets bus authorization after obtaining permission of the master at the time of bus access. MEGA Drive hardware cannot map in SH2 address space. Consequently, MEGA Drive information is indirectly received by communications with the 68000. The 32X has a control register that issues interrupts from 68000 to SH2, a FIFO register that can send data written from the 68000 to the DMA built-in the SH2, and a register that is able to read and write from both the 68000 and SH2, and reads data written from the 68000

SDRAM Component

The 32X has 2 Mbits of SDRAM (synchronous DRAM) as its main memory for the SH2 chips. The SH2 program on the cartridge ROM is loaded in the SDRAM then executed. The SDRAM arranges 16 bytes and reads to the buffer inside the chip, after which, in order to synchronize to the SH2 clock and transfer sequentially, all data after the second data set can be transferred without any restrictions incurred by the operation within the memory. The SH2 is able to rapidly execute data replacement by combining with the SDRAM when cache miss occurs.

Frame Buffer Component

Memory that saves the display contents of one part of the color display is called a frame buffer. For one screen, the display flickers when rewrite does not finish in V Blank (vertical retrace line interval). Therefore, the memory is arranged as two screens in 32X and a method is used to alternately switch between the update screen and display screen. The frame buffer performs the switching operation with each 1 Mbit and program.

VDP Component

32X VDP holds the frame buffer as a control screen and controls the display of the color display. This screen combines MEGA Drive scroll A, scroll B, and sprite as one screen in the front or back. The following three modes can be selected from data formats in the frame buffer.

Direct Color Mode

The direct color mode allocates each of 16 bits to 1 pixel on the screen of which 15 bits is used and indicates any color from 32,768 colors.

Packed Pixel Mode

The packed pixel mode allocates each of 8 bits to 1 pixel on the screen and colors indicated on the color palette mentioned later and indirectly indicated.

Run Length Mode

The run length mode allocates 16 bits as a collection of identically colored pixels that continue with more than 1 pixel in the direction of the scan line. Pixel numbers that are continuous with 8 of the 16 bits and colors indicated on the color palette with the remaining 8 bits are indirectly indicated.

Color Palette Component

The color palette is a 256 word RAM block. When in the packed pixel mode or run length mode, pixel data in the frame buffer selects colors (256 colors from among 32,768 colors) indirectly selected here in advance.

The color selection format is the same whether selecting per frame buffer in the direct color mode, or per color palette in the run-length mode. One color is 16 bits, of which 15 bits are used, and any color can be selected from 32,768 colors. The remaining 1 bit is called a priority-bit (through-bit), pixels indicated by this bit's color are displayed opposite to the MEGA Drive screen. For example, when 32X screens are combined in the rear as a single scroll A, scroll B, and sprite screen, only the pixels that indicated the color of this bit is displayed in front of the MEGA Drive screen.

PWM Component

PWM (Pulse Width Modulation) replaces sampling data with the pulse width and outputs the pulse width. If output is through an integrated circuit the amplitude can be controlled by the pulse width. The 32X can regenerate in stereo PCM wave data converted in advance for PWM.

Chapter 3

Function

Chapter 3 Contents

3.1 Mapping

The 32X hardware can be controlled from both the main CPU SH2 and MEGA Drive 68000. As stated in the last chapter, the layout of each block in the address space of both CPUs is explained here.

MEGA Drive Memory Map

In using the 32X, the exclusive initial program provided by SEGA is laid out cartridge ROM of 3FAH or more and jumped by the reset vector. To map the 32X in 68000 address space, this program sets the ADEN (address enable) bit to 1, initializes the hardware, and executes the application. The figure below shows the 68000 address space immediately after the power is turned on and the initial program executed.

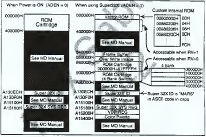

Figure 3.1 MEGA Drive Memory Map

ROM Access When Using the 32X

The 68000 vector area (000000H ~ 0000FFH) is assigned by the custom built-in ROM Because the ROM contents are 00880200H 00880206H, 0088020CH, .., After 880200H (200H of the cartridge ROM), 6-byte JUMP commands are arranged into a jump table

Only when the RV (ROM to VRAM DMA) bit is 1 is it assigned by the cartridge ROM to 100H ~ 3FFFFFH ROM access from the SH2 at this time waits until 68000 rewrites the RV bit to 0.

When the RV bit is 0 access is from 880000H ~ 9FFFFFH to the cartridge ROM 880000H ~ 8FFFFFH is allocated by fixing 000000H ~ 07FFFFH (4 Mbit) of the cartridge ROM. In 900000H ~ 9FFFFFH a cartridge area of 32 Mbits is divided into 4 banks and accessed by the bank set register.

When the 68000 and SH2 are accessed at the same time, the SH2 has priority. Otherwise access is granted on a first come, first served basis the second access waits until the first is over.

When the 68000 and SH2 access the same area at the same time, the SH2 has priority Otherwise access is granted on a first come, first served basis the second access waits until the first is over

The MEGA Drive has a bank set register (A130F1H ~ A130FFH odd numbered addresses) for coping with a cartridge ROM that exceeds 32 Mbits The RV bit should be set to "1" beforehand when accessing here

Access to the 32X VDP

The FM (VDP access authorization) bit must be 0 before the Mega Drive can access the Mars frame buffer, overwrite images VDP register or color palette When the bit is 1, reads are undefined and writes are ignored. Color palette access is words only not bytes

The frame buffer, overwrite image, VDP register, and color palette can be accessed from the MEGA Drive side only when the FM (VDP access authorization) bit is 0 When this bit is 1 reads are undefined, and writes are ignored. Color palette access is in words only not allowing byte access

SH2 Memory Map

The 32X has two SH2 chips mounted to a common bus. Consequently, memory maps of the two chips shown in Figure 3.2 are the same. The SH2 has a built-in cache memory for increasing the speed of command and data accessing. Access of identical components of the 32X can be accessed by two cache/cache through addresses. In cases of the cache address, if is read if data of the address to be accessed is in the cache memory. If not in the cache memory, is read directly from that address, and the cache memory is replaced by the data.

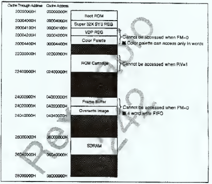

Figure 3.2 SH2 Memory Map

Cache Area Access

Cache memory is memory used for rapidly supplying commands operands and data to the CPU The 32X accesses the cache after commands and data are loaded in the SDRAM In 32X, after having loaded command and data into the SRAM, the catch access is performed The 32X system register and VDP register among others must be cache-through accessed because values through the VDP or other CPU are replaced and the contents of the cache can no longer be guaranteed

Cartridge ROM Access

Only when the RV (ROM to VRAM DMA) bit is 0 can SH2 be accessed to the cartridge RAM When the RV bit is 1 and if accessing from SH2 to the cartridge ROM, a wait occurs until 68000 replaces the RV bit with 0 The RV bit from SH2 can only read

32X VDP Access

Only when the FM (VDP access authorization) bit is 1 can the frame buffer, overwrite images, VDP register, and color palette access from the SH2 side When the FM bit is 0, read is undefined and write is ignored The color palette can access only in words but not in bytes.

The frame buffer and overwrite image have 4 word write FIFO and can write in 3 clock cycles Five clock cycles are required when continuously writing 4 words or more

3.2 Registers

32X registers are classified as shown below Meanings of the address and set value of each register are also shown

32X System Register
[MEGA Drive]

Able to use 32X
- Adapter control register

Issues interrupt for SH2
- Interrupt control register

ROM cartridge bank switching
- Bank set register

Transfers data to SH2 DMAC
- DREQ control register
- 68 to SH DREQ Source Address register
- 68 to SH DREQ Destination Address register
- 68 to SH DREQ Length register
- FIFO register

Refresh signal output to cartridge register
- SEGA TV register

Communication in both directions with SH2
- Communication port register

Control of PWM Sound Source
- PWM Control register
- Cycle register
- L ch pulse width register
- R ch pulse width register
- Mono pulse width register

[SH2]

Interrupt control for SH2
- Interrupt mask register
- H Count register
- VRES interrupt clear register
- V interrupt clear register
- H interrupt clear register
- CMD interrupt clear register
- PWM interrupt clear register

32X custom component activation
- Standby change register

MEGA Drive data received by DMAC of SH2
- DREQ control register
- 68 to SH DREQ Source Address register
- 68 to SH DREQ Destination Address
- 68 to SH DREQ Length register
- FIFO register

Communication in both directions with 68000
- Communication port register

Control of PWM Sound Source
- PWM Control register
- Cycle register
- L ch pulse width register
- R ch pulse width register
- Mono pulse width register

VDP register
    Display mode selection
        Bitmap Mode register

Frame buffer switch
    Frame buffer control register

Screen shift
    Screen shift control register

Data fill for frame buffer
    Auto Fill Length register
    Auto Fill Start Address register
    Auto Fill Data register

[MEGA Drive side]

Using the 32X

- Adapter Control Register (Access Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side	R/W	Read Only													R/W	R/W
A15100H	FM	—	—	—	—	—	—	—	REN	—	—	—	—	—	RES	ADEN

FM VDP Access Authorization
- 0 MD (initial value)
- 1 SH2

REN SH2 Reset Enable
- 0 Disable
- 1 Enable

RES Resets SH2
- 0 Reset
- 1 Cancel reset (initialization by the initial program Change not allowed)

ADEN Adapter Enable Bit
- 0 Prohibits use of 32X
- 1 Permits use of 32X (initialization by the initial program Change not allowed)

Switching access authorization is done while writing to the FM bit Therefore be aware that if writing to the FM bit is done by MEGA Drive while SH2 accesses VDP access authorization is forced to switch to MEGA Drive

Interrupt Issued for SH2

• Interrupt Control Register (Access Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															R/W	R/W
MD Side A15102H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INTS	INTM

INTS Slave SH2 interrupt command
- 0 NO OPERATION (initial value)
- 1 Interrupt command

INTM Master SH2, interrupt command
- 0 NO OPERATION (init value)
- 1 Interrupt command

Both are automatically cleared if SH2 does not interrupt clear

Switches ROM Cartridge Bank

• Bank Set Register (Access Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															R/W	R/W
MD Side A15104H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BK1	BK0

BK1	BK0	Area seen in 900000-9FFFFF
0	0	000000H-0FFFFFH (initial value)
0	1	100000H-1FFFFFH
1	0	200000H-2FFFFFH
1	1	300000H-3FFFFFH

Transfers Data to SH2 DMAC

• DREQ Control Register (Access Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side	Read Only													R/W	R/W	R/W
A15106H	—	—	—	—	—	—	—	—	Full	—	—	—	—	68S	0	RV

Full DMA FIFO Full
- 0 Can write
- 1 Cannot write

RV ROM to VRAM DMA
- 0 NO OPERATION (initial value)
- 1 DMA Start Allowed

The SH2 side cannot access the ROM when RV = 1. (When doing ROM to VRAM DMA, be sure that RV=1) Waits until RV value becomes 0 (RV=0) before accessing

68S	Mode
0	No Operation
1	CPU Write (68K writes data in FIFO)

The internal system starts operation when 68S is 1. Writing 0 force-ends the operation. It is automatically set to 0 after DMA ends.

• 68K TO SH DREQ Source Address Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side	R/W															
A15108H	—								High Order							
A1510AH	Low Order															0

Because the DREQ circuit does not use this data, nothing needs to be set at the time of CPU WRITE.

• 68 TO SH DREQ Destination Address Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side	R/W															
A1510CH	—								High Order							
A1510EH	Low Order															

Sets the SH2 side (SDRAM) address. The DREQ circuit does not use this data. Thus, when the destination address is known beforehand by SH2, or when SH2 doesn't need to know, no settings are needed.

• 68 TO SH DREQ Length Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side	R/W															
A15110H															0	0
															(Fixed)	

Sets the number of data items (unit: word) to be sent to SH2 side. The value to be set is in 4 word units. Low order 2 bit write is ignored (00 fixed). Be sure to set this register for CPU WRITE. At each transfer, this register is decremented and when it becomes 0, the DREQ operation ends. Transfer is done 65536 times when 0 is set. Read time reads the actual count value.

• FIFO Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side	Write Only															
A15112H																

Data is written to this register when DREQ is used by CPU WRITE.

Refresh Signal Output to Cartridge

• SEGA TV Register (Access : Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side																R/W
A1511AH	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CM

CM: Cartridge Mode
0 ROM (initial value)
1 DRAM

This is a SEGA TV exclusive register, use of this bit with other applications is prohibited

Communication in Both Directions with SH2

• Communication Port (Access : Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side								R/W								
A15120H																
A15122H																
A15124H																
A15126H																
A15128H																
A1512AH																
A1512CH																
A1512EH																

This is an 8 word bi-directional register Read/write is possible from both the MEGA Drive and SH2 directions, but when writing the same register from both at the same time, the value of that register becomes undefined Caution is advised

PWM Sound Source Control

- PWM Control Register (Access · Byte/Word)

bit	15	14	13	12	11	10	9	8
MD side					Read Only			
A15130H	—	—	—	—	TM3	TM2	TM1	TM0

	7	6	5	4	3	2	1	0
	Read Only				R/W	R/W	R/W	R/W
	RTP	—	—	—	RMD0	RMD1	LMD0	LMD1

TM3 ~ 0 PWM timer interrupt interval

RTP DREQ 1 occurrence enable (SH2 side only)

0: OFF (initial value)

1 ON

RMD0	RMD1	OUT
0	0	OFF
0	1	R
1	0	L
1	1	Setting not allowed

LMD0	LMD1	OUT
0	0	OFF
0	1	L
1	0	R
1	1	Setting not allowed

Both cannot be set to Lch or Rch

- Cycle Register (Access · Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side					R/W											
A15132H	—															

The base clock frequencies of the cycle registers are fixed respectively NTSC at 23.01 MHz and PAL at 22.8 MHz (set value x Scyc) becomes the cycle

NTSC Scyc = 1/23.01 [MHz] PAL Scyc = 1/22.8 [MHz]

The cycle counter does not operate when both L ch and R ch are off

• L ch Pulse Width Register (Access Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side	Read Only				Write Only											
A15134H	FULL	EMPTY	—													

The value set by bit 11 ~0 x Scyc becomes the pulse width.

FULL: Conditions of pulse width FIFO
- 0 Space available
- 1 No space available

EMPTY: Conditions of pulse width FIFO
- 0 Data per FIFO
- 1 No data per FIFO

• R ch Pulse Width Register (Access Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side	Read Only				Write Only											
A15136H	FULL	EMPTY	—													

See explanation of Lch pulse width register.

• Mono Pulse Width Register (Access Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side	Read Only				Write Only											
A15138H	FULL	EMPTY	—													

See explanation of Lch pulse width register.

If writing to this register, the same value is written to both Lch and Rch.

Note: Bits D0~D11 of all Lch, Rch and MONO pulse width registers are write only. When read is performed undefined data is read. Each PWM of Lch and Rch have three separate FIFO steps.

When both the L and R channels are off, because the cycle counter does not operate, once the FULL bit is set to "1", it will not become "0" as long as the channels are not turned on. When either the L or R channel is on, because the OFF side FIFO is also operating, no sound will be output, however, data within FIFO will disappear. If writing when FIFO is FULL, the oldest data is discarded and shift occurs one item at a time.

[SH2 side]

Interrupt Control for SH2

- Interrupt Mask

(Access : Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side							Read Only	Read Only	R/W				R/W	R/W	R/W	R/W
20004000H	FM	—	—	—	—	—	ADEN	CART	HEN	—	—	—	V	H	CMD	PWM

FM	VDP Access Authorization 0 MEGA DRIVE (initial value) 1 SH2
ADEN	Adapter enable bit 0 the 32X use prohibited 1 the 32X use allowed
CART	Cartridge insert condition 0 Inserted 1 Not inserted
HEN	H INT approval within V Blank 0 H INT not approved (initial value) 1 H INT approved
V	V INT Mask 0 Mask (initial value) 1 Valid
H	H INT Mask 0 Mask (initial value) 1 Valid
CMD	Command Interrupt Mask 0 Mask (initial value) 1 Valid
PWM	PWM timer interrupt mask 0 Mask (initial value) 1 Valid

This register is mapped to the same address for both SH2 master side and slave side. But V, H, CMD, and PWM each possesses exclusive addresses on the master side and the slave side. Other bits are common to both the master and slave sides. Please note carefully that if a "1" is written to the FM bit, access authorization is forced to switch to the SH2 side even if access of VDP is in progress in the MEGA Drive side.

- H Count Register (Access: Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side 20004004H	—								R/W							

Sets H int occurrence interval. Designates by the number of lines.
0 = each line (initial value)

- VRES Interrupt Clear Register (Access: Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side 20004014H	Write Only															

Clears VRES interrupt (interrupt caused by pressing the MEGA Drive reset button). If not cleared, interrupt will no longer occur.

- V Interrupt Clear Register (Access: Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side 20004016H	Write Only															

Clears V interrupt. If not cleared, interrupt will no longer occur.

- H Interrupt Clear Register (Access: Word)

Bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
SH Side 20004018H	Write Only															

Clears H interrupt. If not cleared, interrupt will no longer occur.

• CMD Interrupt Clear Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side 2000401AH	Write Only															

Clears CMD interrupt (command interrupt) If not cleared, interrupt will no longer occur

• PWM Interrupt Clear Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side 2000401CH	Write Only															

Clears PWM interrupt If not cleared interrupt will no longer occur

- Points to be Aware of concerning Interrupt

(1) 32X has VRESINT, VINT, HINT, CMDINT, and PWMINT, but among these only CMDINT has points which differ from other INT. Interrupt is enabled by the Interrupt Mask Register (20004000H) within the SH2 system register, INT occurs, and when INT is masked by the Interrupt Mask Register within the system register before that INT is received, the following will happen

i) VRESINT, VINT, HINT, PWMINT
INT continues to occur until each INT is cleared
ii) CMDINT
INT is negated. But when CMDINT is enabled after CMDINT is not received, CMDINT is again asserted

In short, when all INT occur before they are masked, the INT conditions will continue to be saved as long as that INT is not cleared. But when Interrupt is masked only for CMDINT, INT will temporarily disappear. Still, because CMDINT information will be saved as long as it is not cleared, INT will again occur if CMDINT is enabled.

(2) HEN (HINT authorization bit during V Blank) inside the interrupt mask register of SH2 is common in both Master and Slave. The HINT occurrence interval is affected by this HEN bit.

The value set in the H Count register is enabled, as the next H Blank occurs, after being loaded in the internal counter when H Blank is negated. Also, the internal counter generates HINT as a result of the count, but when H Blank is negated the H Count register value is reloaded. Therefore, when the H Count register is set when H Blank does not occur (because it is not loaded in the internal counter until the next H Blank occurs), HINT may occur according to the value prior to setting the H Count.

ex 1) When H Count register = 0, 1 is set in the H Count register during H Blank. When HEN = 0, HINT occurs within the second H Blank after the existing H Blank is negated.

ex 2) H Count register = 0 and H Count is set to 1 when H Blank does not occur. When HEN = 0, HINT occurs during the next H Blank. HINT occurs during the 2nd H Blank after the H Blank is negated because the H Count register setting (value) is loaded in the internal counter when this H Blank is negated.

Activating the 32X Custom Component

- Stand By Change Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side	Write Only															
20004002H																

Use with system (Boot ROM) Access to this register from the application is prohibited

Receiving MEGA Drive Data by SH2 DMAC

- DREQ Control Register (Access Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side	Read Only													Read Only		
20004006H	FULL	EMPT	—	—	—	—	—	—	—	—	—	—	—	68S	0	RV

Full — Frame Buffer, Write Cache Full
- 0 Space
- 1 No Space

EMPT — Frame Buffer, Write Cache Empty
- 0 Data
- 1 No Data

See explanation of MEGA Drive register for more.

- 68 to SH DREQ Source Address Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side	Read Only															
20004008H	—								High Order							
2000400AH	Low Order															0

- 68 to SH DREQ Destination Address Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side	Read Only															
2000400CH	—								High Order							
2000400EH	Low Order															

See explanation of MEGA Drive side register

• 68 to SH DREQ Length Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side	Read Only															
20004010H															0	0
															(Fixed)	

See explanation of MEGA Drive side register

• FIFO Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side	Read Only															
20004012H																

See explanation of MEGA Drive side register

Communications in Both Directions with 68000

• Communication Port Register (Access Byte/Word)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R/W															
20004020H																
20004022H																
20004024H																
20004026H																
20004028H																
2000402AH																
2000402CH																
2000402EH																

See explanation of MEGA Drive side register

PWM Sound Source Control

- PWM Control Register (Access Byte/Word)

SH side 20004030H	bit 15	14	13	12	11	10	9	8
					R/W	R/W	R/W	R/W
	—	—	—	—	TM3	TM2	TM1	TM0

	7	6	5	4	3	2	1	0
	R/W				R/W	R/W	R/W	R/W
	RTP	—	—	—	RMD0	RMD1	LMD0	LMD1

See explanation of MEGA Drive side register

TM 0 – 3 set the PWM timer interrupt interval and ROM to PWM transfer cycle. Interrupt occurs by cycle register set value x TM cycle When TM = 1 the interval is the same as the cycle register When TM = 0 the interval is 16 times the cycle register

- Cycle Register (Access Byte/Word)

Bit / SH Side	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					R/W											
20004032H	—															

See explanation of MEGA Drive side register

- Lch Pulse Width Register (Access Byte/Word)

Bit / SH Side	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Read Only				Write Only											
20004034H	FULL	EMPTY	—													

See explanation of MEGA Drive side register

- Rch Pulse Width Register (Access Byte/Word)

Bit / SH Side	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Read Only				Write Only											
20004036H	FULL	EMPTY	—													

See explanation of MEGA Drive side register.

• Mono Pulse Width Register (Access : Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH Side	Read Only				Write Only											
20004038H	FULL	EMPTY	—													

See explanation of MEGA Drive side register

VDP Registers (Both MEGA Drive and SH2 Common)

Display Mode Selection

- Bitmap Mode Register (Access Byte/Word)

		Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Read Only								R/W	R/W					R/W	R/W
MD Side	A15180H	PAL	—	—	—	—	—	—	—	PRI	240	—	—	—	—	M1	M0
SH Side	20004100H																

Switching is always allowed but is valid from the next line

PAL TV format
- 0 PAL
- 1 NTSC

Switching is possible only during V Blank

PRI Screen Priority (explained later)
- 0 MEGA Drive has priority (initial value)
- 1 32X has priority

Switching is always allowed, but is valid from the next line

240: 240 Line Mode (Valid only when PAL)
- 0 224 Line (initial value)
- 1 240 Line

M1	M0	Mode
0	0	Blank Mode (initial value)
0	1	Packed Pixel Mode
1	0	Direct Color Mode
1	1	Run Length Mode

Switching is always allowed, but is valid from the next line.

Frame Buffer Switching

- Frame Buffer Control Register (Access Byte/Word)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side	A1518AH	Read Only														R Only	R/W
SH Side	2000410AH	VBLK	HBLK	PEN	—	—	—	—	—	—	—	—	—	—	—	FEN	FS

VBLK:	V Blank 0: During display period 1: During V Blank
HBLK:	H Blank 0: During display period 1: During H Blank
PEN:	Palette Access Approval 0: Access denied 1: Access approved
FEN:	Frame Buffer Access authorization 0: Access approved 1: Access denied
FS:	Frame Buffer Swap 0: Transfers DRAM0 to VDP side (initial value) 1: Transfers DRAM1 to VDP side

- Swapping the Frame Buffer is allowed during V Blank (VBLK = 1) or when in the Blank mode. However, writing the FS bit is always allowed, and when written during display, swapping is done at the next VBlank. With respect to read, the value, which indicates DRAM during display until the next VBlank, is returned.
- When having swapped the Frame Buffer, be sure to access the Frame Buffer after confirming that VBLK=1 or FS bit has changed.
- When having performed FILL, be sure to access the Frame Buffer after confirming that FEN is equal to 0.
- Palette access is possible only during H and V blank.
  Palette can access whenever the bitmap mode is in the direct color mode, as well as during Blank.

Screen Shift

• Screen Shift Control Register (Access Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side A15182H / SH Side 20004102H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SFT (R/W)

SFT Screen 1 dot left shift (explained later)
0 OFF
1 ON
Switching is allowed at any time, but is valid from the next line

Data Fill for Frame Buffer

• Auto Fill Length Register (Access Byte/Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side A15184H / SH Side 20004104H					—				R/W							

Word length when filling DRAM (frame buffer) To set the value, set the value for the to-be-filled word length - 1 (0~255)

Note The Auto Fill function will be explained later

• Auto Fill Start Address Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side A15186H / SH Side 20004106H (R/W)	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1

Sets the start address of the area to be filled A16~A9 remain as fixed, but A8~A1 are incremented at each Fill.

• Auto Fill Data Register (Access Word)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD Side A15188H / SH Side 20004108H	R/W															

Sets data to be filled The Fill operation begins when setting this register

3.3 VDP

32X VDP (referred to as VDP hereafter) controls the color display and has two 1 Mbit frame buffer surfaces for control display screens. Display (to the display screen) is synthesized and composed contextually of a single screen (plane) from these screens and the existing MEGA Drive screen.

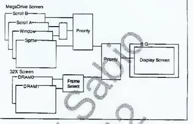

Figure 3.3 Combinations with MEGA Drive Screens

Display Mode

Enables output of images that correspond to the NTSC format (Japan, USA) and the PAL format (Western Europe). When the 32X image output is not blank, the MEGA Drive display mode should select a resolution that is equal to the 32X resolution.

Table 3.1 Display Mode Possible Combinations

32X	MD
Non blank 320 x 224 pixels	Graphic V 40 x 28 cells (320 x 224 pixels)
Non blank 320 x 240 pixels	Graphic V 40 x 30 cells (320 x 240 pixels)
Blank	Graphic IV 32 x 28 cells (256 x 192 pixels) Graphic V 32 x 28 cells (256 x 224 pixels) 40 x 28 cells (320 x 224 pixels) 32 x 30 cells (256 x 240 pixels) 40 x 30 cells (320 x 240 pixels)

VDP Configuration

VDP is mapped, as shown below, from SH2 address 20004100H and 24000000H These exist as I/O devices for the CPU. As a result, accessing without the color palette is only a cache-through address.

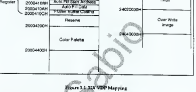

Figure 3.4 32X VDP Mapping

- VDP Register

The VDP register controls RAM block access, the VDP mode, priority, etc The VDP register is read to the VDP display circuit when a horizontal return line is complete Consequently, after the register is set, the settings from the next line become valid for the bitmap mode and screen shift control

- Color Palette

The color palette is RAM block that designates display colors. A cache address is possible This block must always be word accessed

- DRAM

Also called a frame buffer, DRAM stores line tables and bit pattern data for each line Mapping is done for either DRAM 0 or DRAM 1 This block can write in 8-bit or 16-bit widths Write speeds are all the same, but 0 cannot be written in byte access

Over Write Image

Data write can also be done from this area to the frame buffer Because there is specialization in character overwrite, if the significant or insignificant byte of data is 0 when accessing by word, only that part ignores overwrite and holds the original value This block can write in 8-bit or 16-bit widths Write speeds are all the same but 0 cannot be written in byte access

Switching Frame Buffers

By switching the FS bit, the DRAM draw previously handled by the CPU is transferred to the VDP and the contents are displayed In addition, DRAM that has been displayed is mapped instead in the address space, allowing the draw For instance animation can be displayed by switching repeatedly per each single frame (1/60 sec), and for the period equivalent to a single frame (1/60 sec), write process can continue Frame buffer can be switched only in VBlank During display, even when writing to the FS bit, the buffer does not switch until VBlank occurs The FS bit when read, returns the buffer selected on the current display side DRAM access should take place after confirming that VBLK=1, or the FS bit has been switched

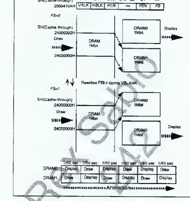

Figure 3.5 Frame Buffer Switch and Animation Display

Color Palette

There is one DRAM0 and DRAM1 common color palette in the 32X, and 0 ~ 255 palette code can be specified per each pixel. The figure below shows the correlation between the color data format, SH2 address, and palette code. Any of R, G, B, each with 5 bits, can be selected from among 32,768 colors.

The color data format is 16-bit and the color for each pixel can be directly selected (when in the direct color mode), but data size can be kept down by indirect-selecting using the 8-bit palette code.

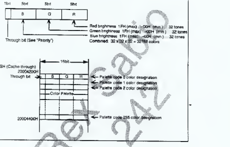

Figure 3.6 Color Data Format and Color Palette

Note: Palette access is possible when PEN = 1 (Frame Buffer Control Register). If accessing when PEN = 0, wait is held until PEN = 1. Also, when PEN goes from 1 ⟶ 0, the written value is not guaranteed. When the color is directly selected, color palette can always be accessed.

Over Write Image

Allows RAM block that is physically identical to the DRAM area to be accessed from this area. When writing data from this area, data on the frame buffer is not changed and remains in its original state when 00H is written in 1 byte units.

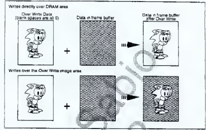

Figure 3.7 Over Write Image

Table 3 2 32X VDP Specifications

Display Size	320 pixels x 224 pixels or 320 pixels x 240 pixels only the non- nterlace mode
Display Colors	32 768 color direct or 256 colors from 32 766 colors (color palette)
Frame Buffer	1 Mbit DRAM x 2 (Line Table Format)
Draw Mode	Direct Color Mode (16 bits/1 pixel 32K color direct) Packed P xel Mode (6 b ts/1 pixel 256 of 32K colors) Run Length Mode (16 bits/continuous same color pixels 256 of 32K colors)
Priority (Comb ne with MEGA Drive screen)	To combine MEGA DRIVE scroll A B and sprites into a single screen 32X screen is synthesized in the front or back
Other	Supports DRAM FILL at VDP side

Line Table Format

There are 256 words in the line table in the frame buffer lead. When writing an address in which pixel data for each line is entered, that line is displayed. The data format following that address can select the three modes explained on the next page. Mode selection is set by combining VDP register bits M1 and M0.

(M1, M0)
= (0, 0) (Blank display)
= (0, 1) Packed pixel mode
= (1, 0) Direct color mode
= (1, 1) Run length mode

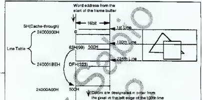

Figure 3.8 Line Table Format

- **Display Precautions**

VDP mechanically displays 320 pixels worth of data from the address specified per the line table. Consequently, caution is required since the overwrite image area data is displayed as is when there is no DRAM area for 320 pixels worth of data after the specified address.

Priority

Select whether or not to use the PRI bit of the VDP register, and whether the 32X screen is to be displayed in front of or behind the MD screen. Also, each through-bit 1-bit is added to the color data. If the PRI bit is used, the pixel that designated the color is displayed in the side opposite of the MD screen. When the MD color code is 0 and when the 32X designates blank by the VDP register each becomes transparent. If both are transparent, the MD background is displayed.

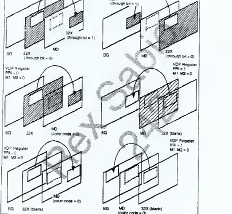

Figure 3 9 Priority

Direct Color Mode

This mode directly expresses data of each line from the pixel in the left corner of the screen by each through-bit B, G R (16-bit). From the size of the frame buffer at 320 words per 1 line,

1 Mbit = 65,536 words ÷ 256 words ÷ 320 x 204 words,

and only 204 lines can be displayed. The number of lines can be increased by making identical line data to be common.

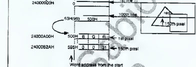

Figure 3.10 Direct Color Mode

Packed Pixel Mode

This mode indirectly expresses data of each line by individual color palette codes (8-bit) from pixels in the left corner of the screen.

Since two pixels are expressed by 1 word, and 1 line contains 160 words,

1 Mbit = 65,536 Words = 256 Words + 160 x 408 Words,

it is possible to have 408 lines of display data.

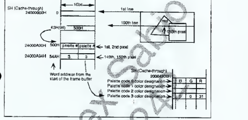

Figure 3.11 Packed Pixel Mode

Screen Shift Control

Because of word units, address data that can be set in the line table can change the table only in 2-dot units when in the packed pixel mode. As a result, use the screen shift control bit (SFT) to change the display position by 1-dot units for horizontal scrolling.

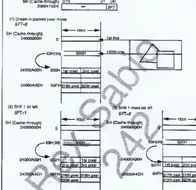

Figure 3.12 Horizontal Scrolling in the Packed Pixel Mode

Run Length Mode

In this mode, pixel data is handled in units as the same colors that continue horizontally, and is represented in palette code (8-bit) and continuing number of pixels = run length data (8-bit). Through-bits are valid in this mode as well. When the run length exceeds 320 pixels for one line of data, the 320 pixels are displayed from the left, and all pixels thereafter are ignored.

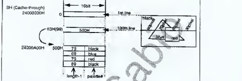

Figure 3.13 Run Length Mode

FILL Function

Auto Fill uses three registers the start address, word length, and file data. VDP begins the fill operation when writing to the file data register. The portion that exceeds the page border is filled from the start of the page. Because VDP and SH2 DRAM accesses conflict while executing Auto Fill, do not access from SH2.

Fill execution time = 7+3 x length (cycle).

After executing Auto Fill, DRAM should be accessed after confirming that VDP register FEN = 0 (completion of frame buffer access via VDP).

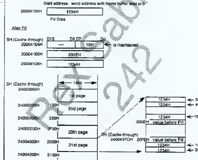

Figure 3 14 Example Executing Fill

Clock Used by the 32X

The master clocks for NTSC and PAL used by the Mega Drive and 32X are different. The 68000 and SH2 system clocks are shown below as standards.

Mega Drive Master Clock Cycle

Mck = 1/fosc [sec]
NTSC fosc = 53.693175 [MHz]
PAL fosc = 53.203424 [MHz]

68000 Clock Cycle

Vclk = 7 Mck, but Mck is the value above

SH2 Clock Cycle

Sclk = Vclk/3, but Vclk is the value above

HBlank and Display Periods

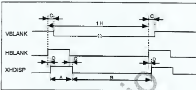

Figure 3.15 HBLANK Period and Display Period

A	Blank Period	100 dot	(860 Mck)
B	Display Period	320 dot	(2560 Mck)
C	HBLANK - VBLANK	27 dot	(224 Mck)
D	HBLANK - XHDISP	3 dot	(24 Mck)

VBlank and Display Periods

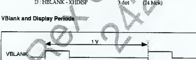

Figure 3.16 VBLANK Period and Display Period

		NTSC	PAL (224)	PAL (240)
A	Blank Period	38H	89H	73H
B	Display Period	224H	224H	240H

VDP Register Latch Timing

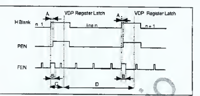

Figure 3.17 VDP Register Latch Timing

A H Blank - PEN	3 dot	(24 Mck)
B FEN Width	40 Sclk	(VDP side refresh)
C H Blank-latch	76 dot	(668 Mck)

The register set within interval C is valid at line n (the nth line), and for interval D is valid at line n+1. Please avoid the type of phenomenon in which the VDP register latch and CPU register access overlap. When the DRAM is being refreshed FEN is 1, but access of the DRAM is possible. Be aware that if 1 is set in 240 bits when in the NTSC mode VDP will have operating errors.

3.4 PWM

PWM Sound Source

32X outputs a 2 ch pulse wave as a sound source. The integrated wave form converts the pulse width to wave height. A variety of sounds can be produced by continuously changing the pulse width

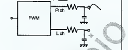

Figure 3.18 32X Sound Source

Figure 3.19 Pulse Wave and Its Integrated Wave Form

Functions of 32X PWM

There are five registers within the SYS REG area for controlling PWM of the 32X (see section 3.2). It is possible to access from both the SH2 and the Mega Drive. Since any register can be accessed in bytes, the Mega Drive side can switch banks and be accessed from the 68000 or Z80.

MD side	SH side	
A15130H	20004030H	PWM Control
A15132H	20004032H	Cycle Register
A15134H	20004034H	L ch Pulse Width Register
A15136H	20004036H	R ch Pulse Width Register
A15138H	20004038H	MONO Pulse Width Register

Figure 3.20 PWM Control Register

32X PWM has the following functions:

- Timer interrupt for SH2
- Can output the same signal as a transfer request (DREQ1) for DMAC built-in SH2.
- L ch and R ch independent output of ON/OFF
- Switches L ch and R ch
- Sampling Rate (pulse output cycle, left right common) variable
- Continuous write of pulse width (pulse width register is 3 step FIFO)

Creating Wave Form Data

Supplied as a Mars sound development tool, the waveform data can be played back by the 32X PWM and output in AIFF (Audio Interchange File Format) using off-the-shelf sampling software and converted through the waveform converter.

Cycle and Pulse Width Settings

Both the cycle and pulse width are 12-bit and can be set from 0 to 4095

The cycle register obtains the required sampling rate with the set value – 1 as a multiple of the base clock cycle When the set value = 0 the cycle is at a maximum (4095 times the base clock cycle) When the set value = 1 (0 times the base clock cycle) PWM will no longer operate and should not be set

When 1047 is set in the cycle register, for example, the base clock for NTSC is 23 01 MHz and the sampling rate is

$$23.01 \times 10^6 \div (1047 - 1) = 22 \times 10^3 = 22 \text{ [kHz]}.$$

In the pulse width register, the height of sample points based on the maximum negative value of the amplitude are written successively Because the set value – 1 is the height, when 1 is set, the maximum negative point of the amplitude is 0, and when 0 is set, the maximum positive point of the amplitude is 4095

The pulse width register is a 3-step FIFO The pulse width is refreshed per each sampling cycle When FIFO is empty, the previous pulse width is held Immediately after reset, FIFO is empty and the pulse width is 0

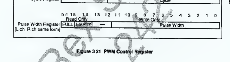

Figure 3 21 PWM Control Register

3.5 SH2

SH2 is a RISC (Reduced Instruction Set Computer) type processor. As with other RISC type processors, it has the following features due to its high speed instruction implementation.

Program (application program) run-time is expressed by the product of the following three elements, C, T, and I

Program run-time = C x T x I
C: cycle number / command, T: cycle time (clock speed),
I: instruction number / task

RISC type processor executes instructions at high speed by reducing C and T.

- Cycle number is reduced per instruction

The conventional CISC (Complex Instruction Set Computer) processor realizes a complex instruction set by micro programs (programs from processor internal instructions). This decoding and run-control is complex and because many execution cycles are needed, SH2 (SH7095) has a simple instruction set with high-speeds by wired logic. Further, by "5 step pipeline control" instruction execution, one instruction is executed in 1 cycle (1 system clock cycle / 23.01 MHz operation time, 43.5 ns) ostensibly by parallel execution of each stage, as shown in the Figure 3.22: instruction 1 "WB", instruction 2 "MA", instruction 3 "EX", instruction 4 "ID", and instruction 5 "IF".

5 Stages of the Instruction Execution

IF	Instruction fetch	Fetch instruction from memory
ID	Instruction decode	Decode fetched command
EX	Instruction execution	Execute decoded contents
MA	Memory access	Access to memory data
WB	Write back	Return memory access results to register

Instruction sequence								
Instruction 1	IF	ID	EX	MA	WB			
Instruction 2		IF	ID	EX	MA	WB		
Instruction 3			IF	ID	EX	MA	WB	
Instruction 4				IF	ID	EX	MA	WB
Instruction 5					IF	ID	EX	MA	WB

Time

Figure 3.22 Pipeline of Instruction Execution

Reduced Cycle Time (Increased Clock Speed)

Internal operations can be made faster if the clock speed of the processor is increased, but a gap is created between main memory access times, a wait state is produced in the processor, and the effective cycle number per one instruction increases. In order to fill in this difference, SH2 has a built-in 4 Kbyte cache memory. The cache shortens access time by 1 line compared to the main memory. When data of the address to access is stored here, the wait state of the processor is reduced because that data is able to be accessed.

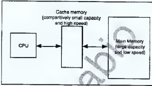

Figure 3.23 Cache Memory

When data accessed by the CPU is stored in the cache memory, it is called *cache hit*, and when not stored in the cache memory is called *cache miss*. For cache miss, a part of the contents of the cache memory is replaced.

Master and Slave

Two SH2 units are packaged on a common external bus in the 32X. SDRAM and 32X hardware resources are connected to this bus and access the periphery while adjusting (bus arbitration) conflicts of the bus One side, the Master mode, releases the bus only when bus authorization is requested from the outside with bus authorization under normal conditions The other side, Slave mode, does not have bus authorization under normal conditions and requests bus authorization each time access to an outside CPU occurs
In a packaged condition, two SH2 units are fixed to the Master mode and Slave mode according to the settings of external pins, and normally the CPU itself is divided by the name "Master" and "Slave "

Note SH2 is able to select a "partial slave mode" by indicating partial space sharing with software from the Master mode but because the necessary outer circuitry is not packaged the Master mode must be used

System performance does not double when two CPUs are used It is less than double for shared parts, such as memory or I/O, due to access competition Accordingly, function fragmentation or bus control that decreases the conflicts is required Within 2 SH2 units, it is normal for the master to control the entire 32X and the slave to restore the computing element inside SH2 and works especially in numerical computing

Master and slave hardware listed below is held separately by the SH2 while everything else is in common

- BOOT ROM
- Interrupt Clear Register
- Bit 0 -3 of the Interrupt Mask Register (V, H, CMD, PWM mask bits)

With the exception of CMD interrupt occurrence (INTM, and INTS bits of the interrupt control register), 68000 does not differentiate SH2 master and slave in terms of hardware

Cache

SH2 contains 4-Kbyte cache memory. Since this memory is accessed per 1 cycle, it is effectively executed by reducing the wait states during accesses to external chips, such as SDRAM, and minimizing command execution pipeline perturbation.

Cache Specifications

- 4-Kbyte, command/data mixed type
- 64 entries x 4-way associative, 16-byte line length (Selection of 64 entries x 2 ways + 2-Mbyte RAM)
- Data write is write-through type, LRU repress algorithm
- Able to select command only/data only repress

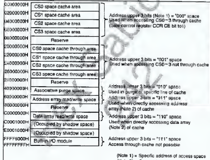

Figure 3.24 Relationship of SH2 Address Space and Cache

Cache Overview

In SH2, address bit 3-0 is called an intra-line byte address, and the cache handles address space from the lead (00000000H) in line units (1 line = 16 bytes). In addition, the address bit 31-29 is called the access space specific address, bit 28-10 is called the tag address, and bit 9-4 is called the entry address.

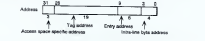

Figure 3.25 SH2 Address

The cache holds command/data from the address array and data array. The data array is 4-way memory in which 64 entries (64 lines), considered as one way, correspond to an entry address. The address array manages the valid/invalid conditions of the held contents and the tag address by entry, way, as well as manages the access order (LRU information) of each way by entry.

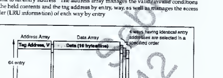

Figure 3.26 Cache Configuration

When reading, the address to be accessed and identical entries are checked all 4-ways and are read from the cache if there are tag addresses that match. If all 4-way tag addresses do not match, they will be selected based upon the LRU information after reading from off-chip memory. Corresponding entry tag address and line data are replaced and output to the CPU upon completion.

When writing, if tag addresses match, data in the cache is rewritten, as well as contents of the memory external to the chip (write-through). If all 4-way tag addresses do not match, they are only stored in the memory external to the chip (off-chip memory).

Cache After Implementing BOOT ROM

The BOOT ROM mounted in the 32X, both master and slave, purges (initializes) and enables the cache immediately after SLEEP from the initial program of the Mega Drive side has been canceled. At this time, 4-way mode, data replace, and command replace can be selected. Initial data is loaded and settings stay unchanged until the application is implemented.

Applications can be executed without tinkering with these settings, but when transferring DMA in the address area where cache is used, the operation can result in differences in the cache memory and external memory contents, and therefore, purge becomes necessary. Purge of all entries, and the purge of a specific line should be differentiated in response to the need.

Purge (Cache Initialization)

Purge of all entries

If "1" is written to the CP bit of the cache control register (CCR), all cache entries will be purged.

Purge of specific lines

In associative purge spaces (40000000H ~ 5FFFFFFFH), the cache address to purge is offset and if write accessed, is checked 4 ways at the same time and only lines that include corresponding addresses are purged. For example, when the slave side cache is purged because contents of the master side 06001004H address are replaced, write access is performed in the 46001004H address by the slave CPU.

DMA

SH2 contains a 2 channel DMA. If transfer request is set to auto request and is within the SH2 address space, transfer between memories can be performed (a generation inside the DMA).

When transfer request is done by an external request (DREQ), DMA transfer ca done by the dual address mode for:

- channel 0 from FIFO to SH2-side RAM;
- channel 1 PWM sound source pulse width register

DMA transfer can be done by the dual address mode. External requests shoul used by the edge trigger, not the level trigger.

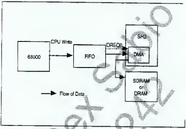

Figure 3.27 DMA between Mega Drive and 32X

DMA transfer from the Mega Drive to 32X is done through the FIFO packaged 32X. If data is set to this FIFO from the Mega Drive, transfer request (DREQ 0) occurs for the DMA of SH2. In the SH2 side, DMA channel 0 is set in external r quest and FIFO is specified and transferred to the source address.

This sets data to FIFO from the Mega Drive side.

CPU Write is the method of writing to FIFO by 68000 directly for each word. A time, if the Full bit of the DREQ control register is 0 write is possible and if Full 1 then it is FIFO Full.

Master-Slave Communication

When communicating for coordination between the master and slave, it is important to know how to properly receive data and take timings

Built-in SCI (Serial Communication I/F)

SH2 has one SCI channel In the 32X, the master and slave are connected to each other making serial communication possible If data receive interrupt is used, timing is effective in severe cases Data is set in the SDRAM described below and timing can be taken by SCI Since the 32X is not equipped with an external clock source for the SH2 SCI an internal clock must be selected Otherwise any setting can be done

SDRAM

This is a wide region able to capture large amounts of data But because the internal operation is in 1 line (=16 bytes) units, transfer of numerical bytes or flag polling is not suitable SH2 does not have a function that combines the cache memory contents of the master and slave As a result, the contents of memories used in common must either be accessed by cache-through or accessed after purging by one CPU when the other CPU is changed

Communication Port

Because there are no SDRAM restrictions when going through the communication port, speed is comparatively rapid even if polling by cache- through. However, large amounts of data cannot be handled since the entire capacity, including communication with the Mega Drive, is eight words

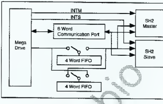

Figure 3.28 68000 and SH2 Communication

Communication Port

The 32X has an 8 word register that can read and write from both "communication ports" used in 68000 and SH2 communication. After the power is turned on, the boot ROM program, following its completion of the initialization and security, notifies the 6000, and as a result, the SH2 master writes "M_OK" (ASCII code 4 bytes) to the start of the communication port, and the slave writes "S_OK" to the 2nd and 3rd words. Communication ports from here after are opened in the application. If simultaneously writing the same register from both 68000 and SH2 or if either the 68000 or SH2 is writing while the other is reading, the value of that register becomes undefined. As a result, dividing the register to be used as SH2 → 68000 and 68000 → SH2 must be avoided.

CMD Interrupt

When timing by both 68000 and SH2, not only can the communication ports be polled together but interrupt can occur from 68000 to SH2. INTM and INTS bits of the interrupt control register correspond to the master side SH2 and the slave side SH2. CMD interrupt occurs if 68000 is set to 1. Interrupt can be cleared if SH2 writes the CMD interrupt clear register. Mask/mask (0/1) cancel can be done by the CMD bit of the interrupt mask register. The CMD interrupt clear register and CMD bit are held separately by the master and slave (addresses are the same). There are no interrupts from SH2 to 68000.

DMA

SH2 has a 2 channel DMA built-in to it When the 32X uses channel 0 from among the two channels, data can be transferred from the Mega Drive side to the SH2 side. The 32X has a DREQ circuit for issuing transfer requests to channel 0 and a FIFO for continuously transferring data. FIFO can be directly written to by the 68000

Interrupt

There are five ways an interrupt can be created

- pressing the Mega Drive reset button
- during vertical feedback
- during horizontal feedback
- interrupt control register write from Mega Drive
- PWM cycle timer

Each interrupt is cleared when written to an interrupt clear register by a different factor. Interrupt continues indefinitely until cleared

Mask/enable is allowed separately by setting the interrupt mask register V, H, CMD, and PWM bits except for the reset button. These four bits have separate registers by master/slave.*

The priority order when using SH2 IRL interrupt (auto vector) is

(Reset button) > (V Blank) > (H Blank) > (Command interrupt) > (PWM cycle timer).

Name	Mask Bit	Level	Interrupt Factor
VRES Interrupt	none	14	Reset button
V Interrupt	V	12	V Blank
H Interrupt	H	10	H Blank
Command Interrupt	CMD	8	Interrupt control register write from MD
PWM Interrupt	PWM	6	PWM cycle timer
	0 Mask, 1 Enable		

* HEN (HITN enable bit inside V Blank) in the interrupt mask register has a common master/slave

Chapter 4

32X Block Access

Chapter 4 Contents

4.1 32X Block Access by SH2

Blocks that Can Be Directly Accessed

Access from SH2, 68000, and Z80 to all 32X buffer registers corresponds to the list below (The √ mark means access from Z80 is possible)

Table 4 1 32X Buffer Register List

Object	Use	Z80	Buffer Register	Description
SH2 Dedicated	SH2 built-in I/O DMA main memory 32X standby Interrupt (mask clear) DMA transfer (receive)		(abbreviated) SDRAM Standby change H Count Interrupt mask VRES Interrupt clear V interrupt clear H interrupt clear CMD interrupt clear PWM interrupt clear DREQ control Reg 68 to SH DREQ Source Address 68 to SH DREQ Destination Address 68 to SH DREQ Length FIFO	Read operation internal 16 byte fixed Boot time custom component H Interrupt interval Use here without mask by SH2 internal Clear interrupt by Mega Drive reset button Clear interrupt from 68000 Sampling data write timing Set "Capture" (See dedication) · · · Transfer request execute to SH2 DMA (read)
68000 Dedicated	32X Use Cartridge ROM access DRAM cartridge Interrupt Execute DMA transfer (send) Write by DMA/CPU	√ √ √ √	Adapter Control Reg Bank Set Reg SEGA TV Reg Interrupt Control Reg DREQ Control Reg 68 to SH DREQ Source Address 68 to SH DREQ Destination Address 68 to SH DREQ Length FIFO	32X is mapped by address space Mapping differs for the single MD Refresh signal output to cartridge Interrupt execute in SH2 Set "Capture" · · · Transfer request execute to SH2 DMA (write)
SH2/ 68000 Common	Communication Sound Graphics	√ √ √ √ √ √ √ √ √	Communication Port PWM Control Cycle Register Lch Pulse Width register Rch Pulse Width register MONO Pulse Width register Bitmap Mode Frame Buffer Control Screen Shift Control Frame Buffer Color Palette Auto Fill Length Auto Fill Start Address Auto Fill Data	Read/Write is possible from both Timer interrupt set for SH2 Sound source sampling cycle Sampling data write · · Packed pixel / Direct color / Run length Draw/Display Switch, see VDP operate status Horizontal scroll of packed pixel mode Draw memory Use when indirectly indicating colors on draw memory Frame buffer data Fill · ·

SH2 Address Space

SH2 divides and manages address space in the four areas from CS0 to CS3, but there is no need for a special awareness that a program has four areas. The system is designed so that a situation in which the area boundary is exceeded and must be continuously accessed is not created. The mapped device can be directly accessed by indicating that address.

Cache-through Access

System and VDP registers must be accessed by cache-through. Although system design also allows access by cache, because there is no guarantee that data of an external device or register which could be re-written by other processors would agree with cache data, purge becomes necessary each time. Therefore, cache can not be used.

VDP Access Competition

When accessing from the SH2 to the VDP register, frame buffer, and color palette, access waits until the FM bit (interrupt mask register bit 15) is 1. After an access series has ended, the FM bit becomes 0 and access authorization changes to 68000. This being the case, SH2 and 68000 wait together until access authorization returns and accesses. When finished, competition can be avoided by returning access authorization to the opponent.

When the FM bit from SH2 is "1", access from 68000 is interrupted by force and the operation that follows is not guaranteed.

ROM Access Competition

SH2 has priority when 68000 and SH2 access the cartridge ROM at the same time. When this happens, the second CPU to be accessed waits until access of the first CPU is finished.

When the 68000 directly accesses contents of the cartridge ROM by the CPU, SH2 can restore high speeds by accessing after the contents of the ROM cartridge is once loaded to the SDRAM. As a result, SH2 accesses ROM data sporadically in certain amounts, whereas ROM access by 68000 occurs regularly. When there is a problem in executing 68000 program interrupted by ROM access wait, the RV bit (DREQ control register bit 0) is set to 1. Here, ROM access from SH2 is in a wait status until 68000 RV = 0. The bit from SH2 is read only.

4.2 32X Block Access by 68000

Blocks That Can Be Directly Accessed

After the power is turned on, address space of 68000 is mapped the same as the Mega Drive unit. If the 32X initial program provided by SEGA is installed following the POWER ON reset vector address, 32X is mapped at the time the execution is transferred to the application program, and is initialized in an access-enabled status.

See Table 4.1 "32X Buffer Register List" in section 4.1 for individual buffer registers.

Cartridge ROM Access When Using the 32X

ROM cartridge 000000H~400000H is mapped unchanged in 68000 address space 000000H~400000H when using the Mega Drive unit. But when using the 32X, mapping is done on and after 880000H when execution is handled by application program.

68000 address	cartridge ROM
880000H~8FFFFFH	000000H~07FFFFH
900000H~9FFFFFH	000000H~0FFFFFH (initial condition)
(4 bank switching)	100000H~1FFFFFH
	200000H~2FFFFFH
	300000H~3FFFFFH

VDP Access Competition

When accessing from 68000 to the VDP register, frame buffer, and color palette, access waits until the FM bit (interrupt mask register bit 15) is 0. After an access series has ended, the FM bit becomes 1 and access authorization changes to SH2. Such being the case, SH2 and 68000 wait together until access authorization returns and accesses. When finished, competition can be avoided by returning access authorization to the opponent.

When the FM bit from 68000 is 0, access from SH2 is interrupted by force and the operation that follows is not guaranteed.

ROM Access Competition

See "ROM Access Competition" in section 4.1.

4.3 32X Block Access by Z80

Blocks That Can Be Directly Accessed

Z80 is loaded as the Mega Drive sound CPU. Even when 32X is mapping in the 68000 address space, 68000 memory area can access each 8000H by switching banks similar to when using the Mega Drive unit. See Table 4.1 "32X Buffer Register List" in section 4.1 for individual buffer registers.

Competition With Other CPUs

Access competition to the 32X block of 68000 and SH2 applies to both Z80 and SH2. See section 4.2 for more information.

Frame Buffer Access

Frame buffer can be written in bytes but data 0 byte write is ignored. (Same for write from both 68000 and SH2)

4.4 Access Timing of Each CPU to 32X Block

The timing sequence when the CPU accesses the peripheral is called a bus cycle, and takes a minimum of 4 Clock with 68000 and 2 Clock with SH2 * In addition, wait time is created on the CPU side due to the difference of the peripheral and operating speeds 1 Wait means that the minimum bus cycle + 1 Clock is necessary in the access A wait is required for all 32X blocks (as shown below) to access from 68000 and SH2 in response to the process contents and operation status

* Besides inputting a Wait signal from the outside, SH2 can input Wait by setting the built-in bus state controller, but after implementing boot ROM only external Wait is set

32X Mode and Cartridge ROM

SH2 (Read/Write)	6 wait (min) ~ 15 wait (max)
68 K (Read/Write)	0 wait (min) ~ 5 wait (max)

Frame Buffer

SH2 (Read)	5 wait (min) ~ 12 wait (max)
SH2 (Write)	1 wait (min) ~ 3 wait (max)
68 K (Read)	2 wait (min) ~ 4 wait (max)
68 K (Write)	0 wait (const)

* Write access to the SH2 frame buffer assumes continuous accessing without an Idle Cycle When the Idle Cycle is inserted between accesses, the next access time is shortened only by the number entered by the Idle Cycle. (The next access time cannot be shorter than a minimum cycle of 3 clock)

A 4 word component of FIFO is held for frame buffer writing Thus, 5 Clock is required if FIFO is FULL and 3 Clock is required if FIFO is not FULL

Palette

SH2 (Read/Write)	5 wait (min) ~ 64 µsec
68 K (Read)	2 wait (min) ~ 64 µsec
68 K (Write)	3 wait (min) ~ 64 µsec

* Wait number 64 µsec means that a wait of a 1 line component display is required (If access to the palette competes with the CPU and VDP, a wait of a 1 line component is required in the CPU side)

VDP Register

SH2 (Read/Write)	5 wait (const)
68 K (Read)	2 wait (const)
68 K (Write)	0 wait (const)

System Register

SH2 (Read/Write)	1 wait (const)
68 K (Read/Write)	0 wait (const)

Boot ROM

SH2 (Read)	1 wait (const)

• SDRAM Access Time

The 32X SDRAM is specialized for the "replace" in the case of the SH2 cache miss, and read transfers in the 8 word burst mode* while write transfers in the 1 word single mode. Access time is fixed at the following values:

Read	12 Clock / 8 Word
Write	2 Clock / 1 Word

* 8-Word burst mode of read is a read operation that takes data in batches of 8 word components from the first address specified by the word address. Because 8 word corresponds to a single line cache, there will be conformity when a cache miss-hit occurs and line data is replaced. But when the SDRAM is read using cache-through, even if the data to be read is only a single word, the access operation to the SH2 SDRAM is 8-word-burst-read-fixed, and action time is required by that amount.

CHAPTER 5

OTHER

Chapter 5 Contents

5.1 Boot ROM

The Boot ROM is an SH2 execution object that is loaded in 32X as ROM, and is different in content with respect to the master CPU and slave CPU. SH2 itself sleeps until activated by the Mega Drive side initial program. After the Boot ROM is reactivated, security (see 6.3 Security) is executed by the master CPU, and if OK, the initial program is executed after the initial data (application program) is loaded from the ROM cartridge to SDRAM.

Initial Data Load

Address 3C0H to 3EDH of the ROM cartridge is called the user header. Shown in Figure 5.1 below are parameters of the initial data load given by the format.

```
*                                                   *
--------------------------------------------------
        MARS User Header ($0003c0)
*                                                   *
--------------------------------------------------

MarsInitHeader
                db      'MARS CHECK MODE'       ; module name
                dl      $00000000               ; version

                dl      $0000c000               ; source address
                dl      $00000000               ; destination address
                dl      $00004000               ; size

                dl      $06000120               ; SH2 (Master) start address
                dl      $06002000               ; SH2 (Slave) start address

                dl      $06000000               ; SH2 (Master) vector base address
                dl      $06002000               ; SH2 (Slave) vector base address
```

Figure 5.1 Example of User Header

The source address is the byte address in which the ROM cartridge lead is 0. The destination address is the byte address in which the DRAM lead is 0. Size is indicated by number of bytes. Because the boot ROM loads the initial data in long word units, an address error will occur if the address is not set by the long word boundaries. Size must be treated in multiples of four. An address error will also occur if the start address and vector base address are not set within the long word boundaries.

Mega Drive and SH2 Synchronization

The Boot ROM flow chart is shown in Figure 5.2. The "comm 0, 4, 8" reference in the figure below refers to communication ports on the 32X. Immediately before an application starts, SH2 master writes "M_OK" (ASCII code 4 bytes) and SH2 slave writes "S_OK" to the communication port. The Mega Drive side executes the initial program (See 5.2 Security) at this time. To be able to synchronize the Mega Drive and SH2 with the application, these must be cleared when moving the Mega Drive side to the application. The SH2 side waits until it is cleared.

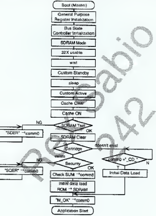

Figure 5.2 Flow Chart of Boot ROM (Master)

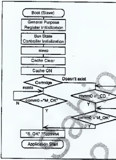

Figure 5.3 Boot ROM Flow Chart (Slave)

5.2 Security

Initial Program

The Initial program performs hardware security and everything required upon resetting in order to equalize all hardware conditions when the Mega Drive and 32X are powered on. In the application program for 32X, the initial program (ICD_MARS PRG) that replaces the one used by the current Mega Drive must be included. This program is executed immediately after the power is turned on or reset by the Mega Drive side. After activating SH2 from the sleep, the Mega Drive and 32X hardware are initialized and their applications executed.

Security

The Initial program must begin from the start of the program (address 3F0H) without change. The Boot ROM built into 32X confirms that the Initial program is provided here. When contents do not match, 32X becomes locked and access cannot be done from the Mega Drive side.

Be aware that release cannot be done if the initial program has been changed or if the initial program is not entered from the start.

Included in the Initial Program

A list of the Mega Drive side sample program is shown in Figure 5.4 below. The initial program (ICD_MARS.PRG) appears in italics.

```
*****************************************************************************
* MARS Sample Program
* Mega Drive Main Routine
* Copyright SEGA ENTERPRISES, LTD 1994
*---------------------------------------------------------------------------*
* CS Hardware R&D Dept
*
*****************************************************************************

*global define
    xref    _colordata,_colorbarcg         ; add.asm
    xref    cramdma,vramdma,vdpinit        ; vdp.h

*include file
    include md.i                ; Mega Drive Map
    include mainwk.ass          ; WorkRAM Assign
    include m_const.ass         ; Constant or Macro

    .symbols
    .list on

*---------------------------------------------------------------------------*
Vector / Mega Drive ID / Mars Initial Program
    include  header.prg                ; Mega Drive & 32X Header
    include  icd_mars.prg              ; Sega Designation: Initial Program & Security
*---------------------------------------------------------------------------*
            bcs     _error0            ; if cs=1 then ID error or Self check error
_init:
            lea     marsreg,a5
```

Figure 5.4 MAINPROG.ASM

5.3 Restrictions

1. When performing SH2 auto request DMA, both master interrupt and slave interrupt must be masked. If DMA is performed by both master and slave at the same time, one side of DMA will perform very slow until the other side of DMA is finished.
2. Since starting the interrupt process may take longer while executing auto request. VDP cannot be accessed within H interrupt while DMA is occurring. When PWM is used, data write may not happen in time. As a result, when either master or slave controls PWM, or when VDP is accessed in H interrupt, auto request DMA cannot be used.
3. Because the time required for the SH2 interrupt to be received depends on the status of the execution, when a high level interrupt is applied following a low level interrupt, the high level interrupt may be received first regardless of the interrupt sequence. Therefore, care is required regarding H interrupt immediately prior to V interrupt and PWM interrupt.

4. When performing CPU write DMA, full bit should be checked for every four words written. This is because the response to the SH2 side DMA may be longer than the 68K access cycle, depending on the access status.

5. When accessing the palette in the packed pixel and run length modes, access needs to be done before 1μs in which the PEN bit changes "1" to "0". Because VDP ignores this access interval, data can not be ensured for both write and read.

Precautions When Using 32X SH2 (SH7095)

If the following operations are performed, the operation that follows can not be guaranteed.

1. Do not use the TAS command with the 32X.
2. Do not use the sleep command in an application.
3. Do not access the bus state controller (FFFFFE0H ~ FFFFFFFFH) in an application.
4. Internal reset should not be done by the "watch dog timer" in an application.
5. Do not access the standby control register (FFFFFE91H) in an application.

In addition, the following conditions exist.

1. Do not manually reset the 32X.
2. NMI is fixed to "H" in the 32X.
   (Items that can be used depending on the development tool also exist.)
3. Serial communication is connected between the master and slave. Because the serial clock is also connected, it can be used in clock synchronization if one side outputs and the other side inputs.

Please make the following setting in response to use when transferring with DMAC of SH2

1 Transfer from DREQ FIFO to memory (channel 0 is used by external request)
DMA Source Address Register 0 (FFFFFF80H)
→ 20004012H fixed
DMA Destination Address Register 0 (FFFFFF84H)
→ optional
DMA Transfer Count Register 0 (FFFFFF88H)
→ same value as DREQ Length Register (20004010H)
DMA Channel Control Register 0 (FFFFFF8CH)
→ 0100 0100 1110 0XXXB (fixed except for X)
DMA Request/Response Select Control Register 0 (FFFFFE71H)
→ 00H fixed
DMA Operation Register (FFFFFFB0H)
→ optional

2 Transfer (channel 1 is used by external request) from memory to PWM FIFO (pulse width register)
DMA Source Address Register 1 (FFFFFF90H)
→ optional
DMA Destination Address Register 1 (FFFFFF94H)
→ 20004034H ~ 20004038H
DMA Transfer Count Register 1 (FFFFFF98H)
→ optional
DMA Channel Control Register 1 (FFFFFF9CH)
→ 00XX 0100 1110 0XXXB (fixed except for X)
or 00XX 1000 1110 0XXXB (fixed except for X)
DMA Request/Response Select Control Register 1 (FFFFFE72H)
→ 00H fixed
DMA Operation Register (FFFFFFB0H)
→ optional

3 Transfer (channels 0, 1 are used by external request) from memory to memory
DMA Channel Control Register 0/1 (FFFFFF8CH/FFFFFF9CH)
→ XXXX XX10 1110 0XXXB (fixed except for X)

Other registers are optional.

Restrictions Concerning SH2 Interrupt

The 32X SH2 has five types of interrupt.

Level 14 VRES interrupt
Level 12 V interrupt
Level 10 H interrupt
Level 8 Command interrupt
Level 6 PWM interrupt

The following restrictions occur when using two or more types of the following interrupts along with interrupts through the SH2 internal peripheral module at the same time

1. There should always be 1 or more interrupt masks. Don't use interrupts of level 15, level 13, level 11, level 9, level 7 and level 1.

2. The SH2 internal free-run-time (FRT) cannot be used with programs. Use the following values in the initial settings

Timer interrupt enable register (TIER)	01H
Output compare register A (OCRA)	0002H
Free run timer control/status register (FTCSR)	01H
Timer control register (TOCR)	E2H

3. External interrupts and the built-in peripheral module interrupt jump destination vector may be mis-recognized. Except for the Non-Maskable Interrupt (NMI) and user brake, interrupt vectors should be set so that they all call the same process routine. At the beginning of this process routine, individual process routines should be called by deciding and branching the SH2 status register values. When the internal peripheral module is assigned the same level as the external interrupt, check the individual interrupt factor flags by the software and find which interrupt occurred.

4. Return from interrupt without doing anything when interrupt levels 15, 13, 11, 9, 7, and 1 occur.

5. Until the RTE command is executed after the external interrupt has been cleared, two or more cycles should be opened. Clearing external interrupt is done by writing to the clear register. When the RTE command is executed, 2 or more commands should be done afterward.

Index